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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>26 June 2007</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-9,11-16,18,19,21-24,26-54 and 57-59</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-9,11-16,18,19,21-24,26-54 and 57-59</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>10 July 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____ .

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____ .

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____ .

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed 6/26/2007 have been fully considered but they are

not persuasive. With respect to amended independent claims 1, 18, 29, 34, 43, 46, 53,

57, Applicant argues: "There is no teaching or suggestion in Phillips of a digital signal

processor "directly coupled" to a digital down converter as recited in the present

independent claims. Rather, Phillips teaches a digital down converter (DDC) 210

directly coupled to a field-programmable gate array (FPGA) 206, and a digital signal

processor (DSP) 216 directly coupled to FPGA 206 or indirectly coupled to FPGA 206

through a bus 218 (see Figures 3A, 8A)." I.e. according to the Applicant, the difference

between the claimed invention, and Phillips et. al., (U.S. 5,859,878) is that Phillips et.

al., teaches the additional component (the FPGA 206 of Fig. 3A) coupled to the DSP

216 and Digital Downconverter (DDC 210), that makes the DSP *indirectly coupled* to the

DDC.

2.   Examiner disagrees with Applicants assessment that there is not suggestion or

motivation to modify Phillips et. al., so that the DSP is *directly coupled* to the DDC (in

Fig 3A for example) without using the FPGA1 block 206. Column 26, lines 29-40

describe the function of the FPGA1 block 206 in Fig. 3A, that is used for control word

formatting (P/S conversion) for communication between the DSP and DDC chips. See

also, lines 32-34 "The disclosed processing architecture permits various methods for

loading these control words depending upon the brand of hardware elements chosen

for the DDC 210 and DSP 216." Clearly, using (or not using) the FPGA1 to format

control words supplied from the DSP to the DDC depends on the brand/make of the

DSP and DDC chips, that is, whether the output word of the DSP is compatible to the

input of the DDC chip. Therefore, at the time of the invention, it would have been

obvious to a person of ordinary skill in the art to modify Phillips et. al., so that the DSP

216 is directly coupled to the digital down converter 210 (of Fig. 3A) when the two

chips have compatible output/input data word formats, i.e when the FPGA component

is not needed since there is not need for data word format conversion between the

DSP and DDC chips.

3.   Therefore, claims 1-9, 11-16, 18-19, 21-52 and 56-59 are rejected under 35

U.S.C 103(a) as being unpatentable over Phillips et. al. (U.S. 5,859,878) in view of

Murphy et. al. ("Satellite-Based Guidance for Precision Approach and Landing of

Commercial Aircraft", 1998 GPS Solutions). The examiner recognizes that obviousness

can only be established by combining or modifying the teachings of the prior art to

produce the claimed invention where there is some teaching, suggestion, **or motivation**

to do so found either in the references themselves or in the knowledge generally

available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed.

Cir. 1992).

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-9, 11-16, 18-19, 21-54, 56-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phillips et. al. (U.S. 5,859,878) in view of Murphy et. al. ("Satellite-Based Guidance for Precision Approach and Landing of Commercial Aircraft", 1998 GPS Solutions).

With respect to claim 1, Phillips et. al. disclose: a front-end circuit operable to receive a plurality of radio signals transmitted across a frequency band and generate an analog signal corresponding within said frequency band (Fig. 3A, front-end includes blocks 102 104 see column 25, lines 31-38 where the AIU receives LOC and GS analog signals from the respective antennas , column 25, lines 47-53 where a NB analog signal is generated); an analog to digital converter coupled to said front-end circuit, said analog to digital converter operable to receive and convert said analog signal to a digital signal (column 25, lines 49-52, narrowband ADC 202 see Fig. 3A); and a digital processing system coupled to said analog to digital converter, said digital processing system operable to receive said digital signal and generate at least one output signal within said frequency band (see Fig. 1, block 106b, also shown in Fig. 3A, see column 23, lines 5-7, 24-28), said digital processing system comprising: a digital down converter (Fig. 3A, block DDC, details shown in Fig. 8A, digital downconverter 210, column 23, lines 5-7, column 26, lines 29-31, the control words are used to frequency control the DDC); a digital signal processor coupled to said digital down converter (Fig.3A,

elements DSP 216, and DDC element 210), said digital signal processor operable to extract information generate said at least one output signal (Fig. 8A, DSP 216, column 10, lines 49-63, decoding operation), wherein said digital signal processor controls said digital down converter (see column 26, lines 41-43, the DSP controls the DDC see also lines 29-31 where control words are used to control frequency translation).

Phillips et. al. do not expressly teach: a digital signal processor directly coupled to said digital down converter; a plurality of channels within said frequency band; a digital processing system operable to generate at least one output signal corresponding to at least one of said plurality of channels; a digital down converter operable to select said at least one of said channels within said frequency band; and a digital signal processor operable to extract said at least information from said at least one of said channels.

With respect to the: a digital signal processor directly coupled to said digital down converter, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify Phillips et. al., so that the DSP 216 is directly coupled to the digital down converter 210 (of Fig. 3A) when the two chips have compatible output/input data word formats (i.e when the FPGA component is not needed, the DSP and DDC are directly coupled).

In the same field of endeavor, Murphy et. al. disclose: a plurality of channels within said frequency band (see page 21, middle of right side column, where in the VHF band (frequency range of 108.10-111.95MHz) exist 40 Localizer channels, see also 40 glideslope channels in another frequency range).

Therefore at the time of the invention, it would have been obvious to a person skilled in the art based on the teachings of Muprhy et. al. that the system of Phillips includes a plurality of channels within said frequency band (40 channels of LO or 40 channels of GS), and therefore it would have been obvious to a person skilled in the art to modify the system of Phillips et. al. so that the a digital processing system is operable to generate at least one output signal corresponding to at least one of said plurality of signals; the digital down converter is operable to select said at least one of said channels within said frequency band; and the digital signal processor operable to extract said at least information from said at least one of said channels, i.e. process the channel out of the 40 channels of the LO or GS received signals that is used, and the motivation to perform the above modification is to extract information from the specific channel (out of the plurality of channel in the frequency band) that is used i.e. contains useful information.

With respect to claim 2, Phillips et.al., further disclose: wherein said digital processing system generates a single output signal comprising a time-domain multiplexed serial data link (see Fig. 8B, (coupled to the system of 8A) where a serial interface is used to supply signals to the computer, see column 7, lines 47-52 , and see Fig. 6, column 23, liens 34-36 where the signal processing (ILS processing) is performed in a TDM fashion).

With respect to claims 3 and 4 all of the limitations of claims 3 and 4 are rejected above in claim 2 (the plurality of signals are generated by the UART and supplied to the plurality of components in computer 112 (the plurality end devices) as shown in Fig.8B).

With respect to claim 5, Phillips et. al., further disclose: wherein said front-end circuit comprises an antenna circuit operable to receive said radio signals (see column 25, lines 36-37 LO, MB, and GS antennas).

With respect to claim 6, Phillips et. al., further disclose: wherein said front-end receiver further comprises an amplifier circuit operable to amplify said received radio signals (column 20,lines 58-67, see signal amplification).

With respect to claim 7, Phillips et. al. further disclose: wherein said front-end circuit further comprises a filter circuit operable to filter said received radio signals (column 20, lines 58-67,line 65 mentions RF filtering).

With respect to claim 8,Phillips et.al., do not expressly teach: wherein said filter circuit comprises a filter selected from the group consisting of high-pass filter, low-pass filter, band-pass filter, notch filter, and combinations thereof.

However to a person skilled in the art at the time of the invention, high-pass filter(s), low-pass filter (s), band-pass filter(s), notch filter(s), and combinations thereof, are known filtering means, therefore it would have been obvious to a person skilled in

With respect to claims 3 and 4 all of the limitations of claims 3 and 4 are rejected above in claim 2 (the plurality of signals are generated by the UART and supplied to the plurality of components in computer 112 (the plurality end devices) as shown in Fig.8B).

With respect to claim 5, Phillips et. al., further disclose: wherein said front-end circuit comprises an antenna circuit operable to receive said radio signals (see column 25, lines 36-37 LO, MB, and GS antennas).

With respect to claim 6, Phillips et. al., further disclose: wherein said front-end receiver further comprises an amplifier circuit operable to amplify said received radio signals (column 20,lines 58-67, see signal amplification).

With respect to claim 7, Phillips et. al. further disclose: wherein said front-end circuit further comprises a filter circuit operable to filter said received radio signals (column 20, lines 58-67,line 65 mentions RF filtering).

With respect to claim 8,Phillips et.al., do not expressly teach: wherein said filter circuit comprises a filter selected from the group consisting of high-pass filter, low-pass filter, band-pass filter, notch filter, and combinations thereof.

However to a person skilled in the art at the time of the invention, high-pass filter(s), low-pass filter (s), band-pass filter(s), notch filter(s), and combinations thereof, are known filtering means, therefore it would have been obvious to a person skilled in

the art at the time of the invention to modify the system of Phillips et. al., to configure

the filter circuit to comprise a band-pass filter since bandpass filters remove unwanted

portions of the RF signal.

With respect to claim 9, Phillips et. al., further disclose: wherein said front-end

circuit further comprises an intermediate frequency mixing circuit operable to translate

said received radio signals to an intermediate frequency band (column 8, lines 36-38,

where IF conversion involves mixing the received RF signals so that they are

downconverted to IF).

With respect to claim 11, the system obtained based on Phillips and Murphy

includes: wherein said digital down converter selects said at least one of said channels

according to configurable channel selection parameters (see column 26, lines 29-31,

41-44, where the configurable parameter is the frequency used for frequency tuning

(during the tune period shown in Fig. 6, see column 23, lines 34-39) to select the LO,

GS channels).

With respect to claim 12, the system obtained based on Phillips and Murphy

includes: wherein said configurable channel selection parameters are software

configurable (see column 22, lines 61-67, column 23, lines 1-4, and column 11, lines 49-

51, where the DSP executes a RAM program to perform the ILC processing the

involves using different tuning frequencies for the LO, GS signals).

With respect to claim 13, all of the limitations of claim 13 are rejected above in claim 11 (see frequency tuning i.e. the channel frequency is changed).

With respect to claim 14, Phillips further discloses: wherein said digital signal processor extracts said information from said at least one of said selected channels according to configurable channel decoding parameters (see column 2, lines 51-56, where received waveforms of various combinations of amplitude, frequency, and phase modulations are processed, see column 21, lines 58-665, where demodulation of any combination of amplitude, frequency, and phase modulation corresponding to the channel decoding parameters, is performed by DSP 216).

With respect to claim 15, Phillips et. al. further disclose: wherein said configurable channel decoding parameters are software configurable (see column 22, lines 61-67, column 23, lines 1-4, and column 11, lines 49-51, where the DSP executes a RAM program to perform the ILC processing including demodulation/decoding).

With respect to claim 16, Phillips et. al., further disclose: wherein said configurable channel decoding parameters are selected from the group consisting of channel frequency, channel modulation scheme, channel bandwidth, channel information format, and combinations thereof (see channel modulation scheme, column

21, lines 58-665, where demodulation of any combination of amplitude, frequency, and

phase modulation).

With respect to claim 18, Phillips et. al. disclose: at least one front-end circuit

group comprising a plurality of front-end circuits (Fig. 3, where the front-end circuit

group is shown as block 103 "AIU" antenna interface unit (including processing prior to

the analog submodule see column 20, lines 58-67) where the AIU includes LOC, MB,

GS antennas (not shown) see column 25, lines 31-41, and these antennas are tuned for

the Localizer, Marker Beacon and Glideslope signals (used for landing) that have

different frequency bands) wherein each of said front-end circuits is operable to receive

a plurality of radio signals transmitted across a frequency band and generate an analog

signal within said frequency band (each one of the three antennas for the LO, MB, GS

signals each one produces analog signals and in each frequency range) at least one

analog to digital converter coupled to said at least one front-end circuit group (see Fig.

8A, block 200 or 202, selection of either the WB ADC converter or NB ADC converter,

either one of the ADC is coupled to the 104 block which in turn is coupled to the AIU as

shown in Fig. 3A), said analog to digital converter operable to receive said analog signal

from said front-end circuits and convert said analog signal to a digital signal (see

column 25, lines 31-40, where the signals out of the antennas (AIUs) can be combined

for further processing into the PCRM (Programmable Common Receiver Module 100)

shown in Fig. 1); and a digital processing system coupled to said at least one analog to

digital converter (Fig. 3A, see functional blocks after digital signal conversion), said

digital processing system operable to receive said digital signal from said analog to

digital converter and generate at least one output signal (see column 25, lines 60-67,

and column 26, lines 1-15, see also column 23, lines 34-39 where the LO, MB, and GS

signals (the specific LO, MB, GS channel in their respective frequency bands) are

processed in a time domain sequence) and ; wherein said radio signals received by any

one of said front-end circuits are within a different frequency band than said radio

signals received by the other of said front-end circuits (see above where the LO, MB,

GS antennas have different ranges corresponding to where the localizer, Marker

beacon, and glideslope signals are located), said digital processing system comprising:

a digital down converter operable to select at least one of said frequencies within said

frequency band of at least one of said front-end circuits (see Fig. 3A, element DDC 210,

and see frequency translation tuning performed by the DDC, column 26, lines 29-32);

and a digital signal processor coupled to said digital down converter (Fig. 3A, DSP, 216,

coupled to DDC 210), said digital signal processor operable to extract infromation from

said at least one of said channels and generate said at least one output signal (see

column 10, lines 49-67, column 11, lines 1-7 see for example message processing

and/or low-data rate speech algorithms performed by the DSP).

Phillips et. al. do not expressly teach: a digital signal processor directly coupled

to said digital down converter; a plurality of channels within said frequency band; a

digital processing system operable to generate at least one output signal corresponding

to at least one of said plurality of channels.

With respect to the: a digital signal processor directly coupled to said digital down

converter, at the time of the invention, it would have been obvious to a person of

ordinary skill in the art to modify Phillips et. al., so that the DSP 216 is directly coupled

to the digital down converter 210 (of Fig. 3A) when the two chips have compatible

output/input data word formats (i.e when the FPGA component is not needed the DSP

and DDC are directly coupled).

In the same field of endeavor, Murphy et. al. disclose: a plurality of channels

within said frequency band (see page 21, middle of right side column, where in the VHF

band (frequency range of 108.10-111.95MHz) exist 40 Localizer channels, see also 40

glideslope channels in another frequency range).

Therefore at the time of the invention, it would have been obvious to a person

skilled in the art based on the teachings of Muprhy et. al. that the system of Phillips

includes a plurality of channels within said frequency band (40 channels of LO or 40

channels of GS), and therefore it would have been obvious to a person skilled in the art

to modify the system of Phillips et. al. so that the a digital processing system is operable

to generate at least one output signal corresponding to at least one of said plurality of

signals; and the digital signal processor operable to extract said at least information

from said at least one of said channels, i.e. process the channel out of the 40 channels

of the LO or GS received signals that is used, and the motivation to perform the above

modification is to extract information from the specific channel (out of the plurality of

channel in the frequency band) that is used i.e. contains useful information.

With respect to claim 19, all of the limitations of claim 19 are analyzed above in claim 18 (see TDM multiplex processing performed during ILS processing, see column 23, lines 34-39).

With respect to claims 21-23, 24, 26, and 27, these claims are rejected based on a rationale similar to the one used to reject claims 5-7, 9, 11, and 14 respectively.

With respect to claim 28, the system obtained based on Phillips and Murphy does not expressly teach: comprising a plurality of front-end circuit groups and a plurality of corresponding analog to digital converters, wherein said digital processing system is operable to receive a plurality of digital signals from said analog to digital converters and generate at least one output signal corresponding to at least one of said channels within said frequency band of at least one of said front-end circuits of at least one of said front-end circuit groups.

However, at the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Phillips and Murphy, so that it comprises a plurality of front-end circuit groups (instead of the one circuit group (receiving signals LO, GS) which is taught by Phillips and Murphy, two circuit groups each of which receives signals LO, GS (duplicate circuit)) of the circuit group taught by Phillips and Murphy) and a plurality of corresponding analog to digital converters, wherein said digital processing system is operable to receive a plurality of digital signals from said analog to digital converters and generate at least one output signal corresponding to at

least one of said channels within said frequency band of at least one of said front-end

circuits of at least one of said front-end circuit groups (duplicates of the processing

components up to digital submodule 106b of Fig. 1 corresponding to the duplicate

second front-send circuit group).

The motivation behind such a modification is that a plurality (two) front-end

circuit groups (and A/D) would have been obvious to a person skilled in the art as a

back-up front-end circuit group and A/D converter, in case a malfunction of the first

front-end circuit group and A/D converter occurs.

With respect to claim 29, claim 29 is rejected based on a rationale similar to the

one used to reject claim 18 above, and with respect to the limitation: "…a plurality of

analog to digital converter each of which is coupled to at least one of said front end

circuit…" see Fig. 3A of Phillips where two ADC are shown 200 (wide band ADC), and

202 (narrowband ADC) converting either the received narrowband or wideband signals

(not at the same time though).

With respect to claims 30-31, these are rejected based on rationale similar to the

one used to reject claims 22-23 above.

With respect to claim 33, Phillips further discloses: wherein at least one of said

analog to digital converters is operable to receive analog signals from a plurality of front-

end circuits and convert said analog signals to a digital signal (see column 19, lines 65-

67, where ILS processing (see column 22,lines 62-64 involving signals LOC, MB, GS

from respective antennas) is narrowband i.e. the NB ADC is used).

With respect to claims 34, 35, 36, 37, 38, 39, 40, 41-42, these claims are rejected

based on a rationale similar to the one used to reject claims 18, 22, 23, 24, (27), 2, 3,

4,4, respectively.

With respect to claim 43, Phillips discloses: a plurality of front-end circuits (Fig. 3,

where the front-end circuit group is shown as block 103 "AIU" antenna interface unit

(including processing prior to the analog submodule see column 20, lines 58-67) where

the AIU includes LOC, MB, GS antennas (not shown) see column 25, lines 31-41, and

these antennas are tuned for the Localizer, Marker Beacon and Gliseslope signals

(used for landing) that have different frequency bands) each of which is operable to

receive a plurality of radio signals transmitted across a frequency band and generate

analog signals that are combined into a composite analog signal corresponding within

said frequency band (see column 25, lines 39-41, see addition of antenna inputs

(analog singals)); a single analog to digital converter operable to receive the composite

analog signal and convert the composite analog signal to a single digital signal (see

column 25,lines 50-52, the NB ADC is used); a digital processing system operable to

receive said digital signal from said analog to digital converter and generate at least one

output signal within said frequency band (see column 25, lines 60-61 the ILS processing

and column 23, lines 124-36, digital processing of ILS signals), said digital processing

system comprising: a digital down converter operable to select said at least one

frequency with said frequency band (see Fig. 3A, element DDC 210, and see frequency

translation tuning performed by the DDC, column 26, lines 29-32); and a digital signal

processor coupled to said digital down converter (Fig. 3A, DSP 216 and DDC 210 are

coupled), said digital signal processor operable to extract information from said at least

one of frequencies and generate at least one output signal (see column 10, lines 49-67,

column 11, lines 1-7 see for example message processing and/or low-data rate speech

algorithms performed by the DSP).

Phillips et. al. do not expressly teach: a digital signal processor directly coupled

to said digital down converter corresponding to a plurality of channels within said

frequency band; a digital processing system operable to generate at least one output

signal corresponding to at least one of said channels.

With respect to the: a digital signal processor directly coupled to said digital down

converter, at the time of the invention, it would have been obvious to a person of

ordinary skill in the art to modify Phillips et. al., so that the DSP 216 is directly coupled

to the digital down converter 210 (of Fig. 3A) when the two chips have compatible

output/input data word formats, (i.e when the FPGA component is not needed, the DSP

and DDC are directly coupled).

In the same field of endeavor, Murphy et. al., disclose: a plurality of channels

within said frequency band (see page 21, middle of right side column, where in the VHF

ban (frequency range of 108.10-111.95MHz) exist 40 Localizer channels, see also 40

glideslope channels in another frequency range).

At the time of the invention, it would have been obvious to a person skilled in the

art based on the teachings of Muprhy et. al. that the system of Phillips includes a

plurality of channels within said frequency band (40 channels of LO plus the 40

channels of GS since the signals are combined), and therefore it would have been

obvious to a person skilled in the art to modify the system of Phillips et. al. so that the a

digital processing system is operable to generate at least one output signal

corresponding to at least one of said plurality of signals; and the digital signal processor

operable to extract said at least information from said at least one of said channels, i.e.

process the channel out of the 40 channels of the LO (or the 40 GS channels) received

signals that is used, and the motivation to perform the above modification is to extract

information from the specific channel (out of the plurality of channel in the frequency

band) that is used i.e. contains useful information.

With respect to claim 44, claim 44 Phillips discloses: wherein said output signal

comprises a time-domain multiplexed serial data link (see column 23,lines 34-37 and

Fig. 6 where the signals are processed in a time-domain multiplex fashion and therefore

the output of the digital processing system is also TDM).

With respect to claim 45, Phillips further discloses: further comprising means for

generating a plurality of signals from said time-domain multiplexed serial data link for

transmission to a plurality of end devices (Fig. 8B, serial interface 114 (UART), see

column 12, lines 60-67, also column 7, lines 47-55, where the plurality of signals are the

signals out of the serial interface (UART) transmitted to the various computer

components as shown in Fig. 8B).

With respect to claim 46 claim 46 is rejected based on a rationale similar to the

one used to reject claim 1 above, and Murphy et. al.., further disclose: wherein said

frequency band comprises aviation band radio signals (see middle of right side column

on page 21, where the aviation signals (referred to as LO in the Phillips et.al. reference

)(see localizer frequency band 108.10-111.95MHz) and Glide slope (GS in the Phillips

et. al. reference) spans 326.6-335.4Mhz frequency range).

With respect to claim 47, Murphy et. al. further disclose: wherein said aviation-

band radio signals comprise aviation navigation radio signals (see right side column of

page 21, where the localizer provides navigation information about the runway center

line).

With respect to claim 48, Phillips et. al. further disclose: wherein said aviation-

band radio signals comprise aviation communication radio signals (see column 2,lines

51-55, and see column 39, lines 56-66, where the VHF-AM signal is a communication

signal).

With respect to claim 49, claim 49 is rejected under a rationale similar to the one used to reject claims 47 and 49.

With respect to claims 50-52, these claims are rejected based on a rationale similar to the one used to reject claims 2-4 respectively.

With respect to claim 53, claim 53 is rejected based on a rationale similar to the one used to reject claim 22 above and Phillips discloses the limitation: "wherein said radio signals comprise aviation navigation and aviation communication radio signals" (see column 2, lines 51-56, received analog waveforms include (aviation) communication and navigation signals, (i.e. aviation cni signals)).

With respect to claim 54, claims 54 is rejected based on a rationale similar to the one used to reject claim 19 above.

With respect to claim 57, claim 57 is rejected based on rationale similar to the one used to reject apparatus claim 53 above (assuming one front-end circuit group that comprises a plurality of front-end circuits)).

With respect to claim 58, Phillips further discloses: further comprising mixing said received radio signals to an intermediate frequency band (column 8, lines 36-38, where

IF conversion injvolves mixing the received rf signals so that they are downconverted to

IF).

With respect to claim 59, Phillips further discloses: wherein said output signal is

generated by: applying software configurable channel selection parameters to said

digital signal to select at least one of said digitized channels within said frequency band;

extracting information from said at least one of said selected digitized channels

according to software configurable channel decoding parameters; and conveying said

extracted information within said output signal.

Conclusion

6.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272

5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

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USPTO Customer Service Representative or access to the automated information

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SV
8/1/2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER